IN THE CLAIMS:

Please cancel claims 1, 8-9, 12-14, and 17-18 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown in the following claims listing.

1-18. (Cancelled)

19. (Currently amended) A system, comprising:

a node including a processing subsystem and an interface coupled by an address network and a data network;

an additional node including an additional processing subsystem and an additional interface coupled by an additional address network and an additional data network;

an inter-node network configured to convey communications between the node and the additional node, wherein the interface and the additional interface are coupled to send and receive communications on the inter-node network;

wherein the processing subsystem is configured to transition an access right to a coherency unit in response to receiving a data packet, including requested data, on the data network and to transition an ownership responsibility for the coherency unit in response to receiving a corresponding address packet on the address network;

wherein the corresponding address packet and the data packet are part of a read-to-own transaction initiated by the processing subsystem;

wherein the interface within the node is configured to delay providing the data packet on the data network until the interface receives an indication from the additional interface via the inter-node network that any shared copies of the coherency unit in the additional node have been invalidated;

wherein in response to receiving the address packet via the address network, a memory subsystem included in the node is configured to send [[a]] another data packet indicating the read-to-own transaction to the interface, wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the another data packet indicating the read-to-own transaction; and

wherein the additional interface is configured to receive the read-to-own message via the inter-node network and to responsively send an invalidating address packet on the additional address network, wherein in response to the additional processing subsystem having an access right to but not an ownership responsibility for the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to the invalidating address packet.

20. (Previously presented) The system of claim 19, wherein the transaction also includes an additional address packet sent on the additional address network and at least one message sent on the inter-node network.

21. (Cancelled)

22. (Previously presented) The system of claim 20, wherein the additional interface is configured to broadcast an invalidating address packet on the additional address network in response to receiving a message indicating the transaction from the interface via the inter-node network.

23. (Previously presented) The system of claim 20, wherein the additional interface is configured to send an acknowledging message to the interface via the inter-node network in response to the additional interface receiving the invalidating address packet on the additional address network, wherein the acknowledging message includes the indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein if the additional processing subsystem has an access right to but not ownership of the coherency unit, the additional processing subsystem is configured to transition the access right to the coherency unit upon receipt of the invalidating address packet.

24. (Original) The system of claim 20, wherein the transaction is a read-to-own transaction, wherein the processing subsystem is configured to initiate the read-to-own transaction by sending a read-to-own packet on the address network.

25. (Original) The system of claim 24, wherein no memory subsystem included in the node maps the coherency unit;

wherein in response to the read-to-own packet on the address network, the interface is configured to send a read-to-own message to the additional interface in the additional node.

26. (Original) The system of claim 19, wherein the address network is configured to convey the address packet from a directory to the processing subsystem in point-to-point mode.

27. (Original) The system of claim 19, wherein the address network is configured to convey the address packet in broadcast mode.

28-34 (Cancelled)

35. (New) A system, comprising:

a node including a processing subsystem, a memory subsystem, and an interface coupled together by an address network and a separate data network; and

an additional node coupled to the node by an internode network, wherein the additional node includes an additional processing subsystem and an

additional interface coupled together by an additional address network and an additional data network;

wherein as part of a coherency transaction involving a coherency unit cached by the processing subsystem, the processing subsystem is configured to initiate a read-to-own transaction by sending an address packet for the coherency unit onto the address network;

wherein the memory subsystem is configured to send a data packet, via the data network, indicating the read-to-own transaction to the interface in response to receiving the address packet;

wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the data packet indicating the read-to-own transaction;

wherein the additional interface is configured send an invalidating address packet on the additional address network in response to receiving the read-to-own message, wherein in response to the additional processing subsystem having an access right to, but not an ownership responsibility for, the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to receiving the invalidating address packet, wherein the additional interface is further configured to send, via the internode network, an indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein the interface is configured to delay providing to the processing subsystem another data packet including requested data on the data network until the interface receives the indication; and

wherein the processing subsystem is configured to transition an ownership responsibility for the coherency unit in response to receiving a response address packet on the address network, and to transition an access right to the coherency unit in response to the processing subsystem receiving the another data packet.

36. (New) The system of claim 35, wherein the interface is configured to forward the read-to-own message to the additional interface via the inter-node network in response to receiving the address packet.

37. (New) The system of claim 36, wherein the coherency unit is not mapped by any memory subsystem included in the node, and wherein the additional node is a home node for the coherency unit.

38. (New) The system of claim 35, wherein if the additional processing subsystem has an ownership responsibility associated with the coherency unit, the additional interface is configured to send an additional address packet on the additional address network, and the additional processing subsystem is configured to transition the ownership responsibility to the coherency unit upon receiving the additional address packet.

39. (New) The system of claim 38, wherein the additional processing subsystem is configured to send a data packet corresponding to the coherency unit to the additional interface in response to receiving the additional address packet, wherein the additional processing subsystem is configured to transition an access right associated with the coherency unit in response to sending the data packet corresponding to the coherency unit.

40. (New) The system of claim 35, wherein the data packet indicating the read-to-own transaction is report (REP) data packet.

41. (New) The system of claim 35, wherein the address network is configured to convey the address packet in point-to-point mode.

42. (New) The system of claim 37, wherein the address network is configured to convey the address packet in broadcast mode.